

REMARKS

In the Office Action, Claims 1-28 were examined and are rejected. In response to the Office Action, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-28 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1-19 and 21-27 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,949,280 issued to Littlefield ("Littlefield"). Applicants respectfully traverse this rejection.

Regarding Claims 1 and 6, Claims 1 and 6 recite the following claim features, which are neither disclosed nor suggested by Littlefield:

enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and
granting the processing element ownership over the selected hardware accelerator. (Emphasis added.)

According to the Examiner, the above recited features of Claims 1 and 6 are anticipated by Littlefield. For at least the reasons described below, Applicants respectfully submit that Littlefield fails to disclose, teach or suggest the above recited features of Claims 1 and 6.

In contract to the above recited features of Claims 1 and 6, Littlefield discloses a parallel processor based raster graphic system architecture. As disclosed by Littlefield, the processing of graphic commands, the transferring of pixel data into a frame buffer, the rate at which the frame buffer can transfer pixel data to the display device as well as communications between units of a host computer and a graphic system can each create a potential bottleneck in generating raster images. (See col. 1, lines 34-43.) As disclosed by Littlefield:

To eliminate the bottlenecks, a system architecture is needed that allows unrestrained mapping of any graphics processor output to any pixel in the graphics display. Each graphics processor within the system must be able to process any

part of the graphics commands stream from the host computer and transfer the resulting pixel data to the appropriate pixel location in the frame buffer without delay. (Col. 3, lines 41-48.) (Emphasis added.)

To provide the system architecture referred to by Littlefield, Littlefield discloses an interconnection network. As disclosed by Littlefield:

The interconnection network comprises a packet switching network. The graphics processors are adapted to transmit the pixel data in addressed data packets to the interconnection network for routing to the addressed parts of the frame buffer. The network itself comprises a plurality of routing nodes providing a route from each graphics processor to any part of the frame buffer. (col. 4, lines 21-28.) (Emphasis added.)

The interconnection network referred to by Littlefield is illustrated with reference to Fig

3. As disclosed by Littlefield:

the network 18 comprises a packet switching network having three levels of network nodes. Packets containing destination address (i.e., pixel location) and corresponding data (e.g., function code, pixel value, Z-value) are prepared by the graphics processors 12 and sent into the network 18 along input data paths. At each node 22 within the network 18, the address field of a packet is examined to determine the routing to the appropriate memory location in the frame buffer 14. (col. 6, lines 31-39.) (Emphasis added.)

According to the Examiner:

Littlefield teach a system as shown in FIG 5, comprising a plurality of processing elements (29) of a media signal processor 28, a selection unit (interconnection network 18), a plurality of hardware accelerators (12), a memory interface 18, and a random access memory 14 coupled to the memory interface. (pg. 2, ¶ 4 of the Office Action mailed 06/28/2006.)

As disclosed by Littlefield:

A second embodiment of the host interface is shown in FIG 5, for use with a multiprocessor host 28. The graphics system 10 therein is driven by the host 28 via multiple data paths each with a separate graphics command stream. A second interconnection network 18 can be utilized to connect each application processor 29 within the host 28 with any of the graphics processors 12. In the simplest case, the interface can be eliminated and each application processor 29 within the host 28 is paired with a graphics processor 12. (col. 7, lines 19-28.) (Emphasis added.)

Although Littlefield discloses that second interconnection network 18 may be used to connect each processor 29 within host 28 with any of the graphic processor 12, as taught by Littlefield. In the simplest case, such interface can be eliminated and each application processor 29 within the host 28 is paired with a graphics processor 12. (See supra.) Applicants respectfully submit that application processors 29 of host application 28 do not set a bit of a register in order to receive ownership of a specific one of the graphic processors (GP) 12, as shown in FIG 5. Furthermore, as disclosed by Littlefield, in the embodiment shown in FIG 4, the graphics processors are assigned according to a first free bases.

Consequently, Applicants respectfully submit that based recited on the passages above assuming each application processes 29 of host 28 can connect with any graphics processors 12, Littlefield fails to teach how an application processor 29 select the respective graphics processor GP 12 as shown in FIG 5. According to the Examiner:

Littlefield teach enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of register within the register file (in the form of a packet) set by a processing element, and granting the processing element ownership over the selected hardware accelerator (col. 8, lines 40-60.) (Supra. lines 5-9.)

As indicated with regard to the passages referred to by the Examiner:

The shift register for each input port is coupled to multiplexors 42 and 44 so that the input data can be routed to either shift register for transfer through an associated output port. Output port selection is determined by the packet address bits that are read by routing arbitration logic 45 which controls the routing of data through multiplexors 42 and 44. (col. 8, lines 45-51.) (Emphasis added.)

As mandated by case law, “Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.” Lindermann Maschinenfabrik v. American Hoist & Derrick (“Lindermann”), 730 F.2d 452, 1458 (Fed. Cir. 1994) (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner (“Banner Titamium”), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, the disclosure of Littlefield is directed to the programming of packet address bits of a packet (set by a graphics processor 12) and the packet is transmitting into the network 18 along

input data paths since the address field of the packet is examined and determines the routing to the appropriate memory location of the frame buffer (see col. 6, lines 31-38.)

Applicants respectfully submit that the disclosure of Littlefield fails to disclose, teach or suggest how an application processors (AP) 29 of host application 28 populates the address field of a packet to determine the routing to the appropriate graphics processor or GP 12, as shown in FIG 5. Accordingly, Applicants respectfully submit that the capability disclosed by Littlefield to enable connection between any AP 29 and any GP 12 via interconnection network 18 neither discloses, teaches or suggests enabling a hardware accelerator from a plurality of hardware accelerators according to at least one bit of register within the register file set by a processing element.

Applicants respectfully submit that the disclosure within Littlefield regarding packets containing destination addresses that are examined to determine the routing of the packet to the appropriate memory location in the frame buffer 14 (see col. 6, lines 31-38) fails to disclose, teach or suggest the granting of ownership of a hardware accelerator to a processing element according to the at least one bit of register within a register file set by the processing element, as recited by Claims 1 and 6. Consequently, Applicants respectfully submit that the failure of Littlefield to provide a disclosure, teaching or suggestion regarding the capability of AP 29, as shown in FIG 5, to connect with a GP 12, as shown in FIG 5, prohibits the Examiner from illustrating that Littlefield teaches or suggests granting the processing element ownership over a selected hardware accelerator according to the setting of at least one bit of a register within the register file set by the processing element to select the hardware accelerator, as recited by Claims 1 and 6.

Accordingly, Applicants respectfully submit that the Examiner is prohibited from relying on Littlefield as an anticipatory reference since Littlefield fails to exactly disclose each and every element recited by Claims 1 and 6. Banner Titanium, supra. Hence, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation of Claims 1 and 6 since the Examiner fails illustrate that the single prior art reference disclosure of Littlefield includes the presence of each and every element recited by Claims 1 and 6, and as arrange in such claims. Lindermann, supra.

Consequently, Applicants respectfully submit that Claims 1 and 6 are patentable over Littlefield, as well as references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 1 and 6.

Regarding Claims 2-5 and 7-10, Claims 2-5 and 7-10, based on their dependency from Claims 1 and 6, respectively, are also patentable over Littlefield, as well as references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 2-5 and 7-10.

Regarding Claims 11 and 21, Claims 11 and 21 recite the following claim feature, which is neither disclosed, taught nor suggested by Littlefield, as well as references of record:

a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators, the selection unit and the plurality of processing elements, at least one of the general purpose registers including at least one bit to allow a processing element to select a hardware accelerator; and

a control unit to direct the selection unit to activate the selected hardware accelerator to grant the processing element ownership over the selected hardware accelerator. (Emphasis added.)

Applicants respectfully submit that the above-recited features of amended Claims 11 and 21 are analogous to the above-recited features of Claims 1 and 6. Consequently, Applicants' arguments provided above with regard to the §102(a) rejection of Claims 1 and 6 as anticipated by Littlefield equally apply to the Examiner's §102(a) rejection of Claims 11 and 21.

Applicants respectfully submit that Littlefield fails to disclose a register file, as recited by amended Claims 11 and 21. For the reasons indicated above, Littlefield fails to disclose that an AP 29 sets a bit within a file to select a GP 12 (see FIG 5.) Furthermore, Applicants respectfully submit that the setting of an address field of packets to route the packets to a selected memory location in Frame Buffer 14 does not disclose a register file, as recited by Claims 11 and 21.

Furthermore, Littlefield fails to disclose either the selection units or control units, as recited by amended Claims 11 and 21, where the control unit directs the selection unit to activate a selected hardware accelerator to grant a processing element ownership of the selected hardware accelerator. Consequently, Applicants respectfully submit that the single prior art of reference

disclosure of Littlefield fails to include the presence of each recited feature of Claims 11 and 21, as required to establish a *prima facie* case of anticipation. Lindermann, supra.

Accordingly, amended Claims 11 and 21, for at least the reasons provided above, are patentable over the combination of Littlefield. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 11 and 21.

Regarding Claims 12-20 and 22-28, Claims 12-20 and 22-28, based on their dependency from Claims 11 and 21, respectively, are also patentable over Littlefield. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 12-20 and 22-28.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 27 and 28 under 35 U.S.C. §103(a) as being unpatentable over Littlefield. Applicants respectfully traverse this rejection.

Regarding Claims 27 and 28, Claims 27 and 28 depend from Claim 21. Applicants respectfully submit that for at least the reasons provided above, Littlefield fails to either disclose, teach or suggest the register file as recited by Claim 21, which includes at least one general purpose registry including at least one bit to allow a processing element to select the hardware accelerator, as well the control unit to direct the selection units to act as the hardware accelerator to grant the processing element ownership over the selected hardware accelerator, as recited by Claim 21.

Accordingly, Applicants respectfully submit that Claim 21 is patentable over Littlefield, as well as references of record. Therefore, Claims 27 and 28, based their dependency on Claim 21, are also patentable over Littlefield, a well as references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 27 and 28.

The Examiner has rejected Claim 20 under 35 U.S.C. §103(a) as being unpatentable over Littlefield in view of U.S. Patent No. 6,477,177 issued to Potts ("Potts"). Applicants respectfully traverse this rejection.

Regarding Claim 20, Claim 20 depends from Claim 11. Regarding the Examiner's citing of Potts, Applicants respectfully submit that the Examiner's citing of Potts fails to rectify the deficiencies of Littlefield in failing to either disclose, teach or suggest whether an AP 29 of host application 28 includes the capability to select the specific GP or graphics processor 12 of graphics system 10 as shown in FIG 5. Although Littlefield teaches that interconnection network enables connection of an AP 29 to any one of the GP 12, Littlefield fails to provide any disclosure, teaching or suggestion with regard to how an AP 29 would direct the interconnection network 18 to provide a connection with a requested GP of the plurality of GP 12, as shown in Fig 5.

Consequently, Applicants respectfully submit that Claim 11 is patentable over the combination of Littlefield in view of Potts, as well as references of record. Therefore, Claim 20, based on its dependency from Claim 11, is also patentable over the combination of Littlefield in view of Potts as well as references of record.

Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-28 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: Sep 26, 2006

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Annie McNally

09/26/2006
Date